| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L2 | 21 | (single adj2 chip) same core same peripheral same programmable | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/12/20 08:15 |
| L3 | 6 | parameter and 2 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/12/20 08:15 |
| S1 | 1960 | programmable adj2 chip | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:29 |
| S2 | 4 | (programmable adj2 chip) same core same peripheral | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:34 |
| S3 | 19 | (single adj2 chip) same core same peripheral same programmable | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/12/20 08:14 |
| S4 | 6464 | uart | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:40 |
| S5 | 248365 | timer | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:40 |
| S6 | 869492 | interface | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:40 |
| S7 | 165 | custom$3 adj2 peripheral | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:46 |

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| S8 | 4577 | wizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 07:56 |
| S9 | 1 | ((single adj2 chip) same core same peripheral same programmable) and uart | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:42 |
| S10 | 8 | ((single adj2 chip) same core same peripheral same programmable) and timer | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:42 |
| S11 | 16 | ((single adj2 chip) same core same peripheral same programmable) and interface | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:43 |
| S12 | 8 | (((single adj2 chip) same core same peripheral same programmable) and timer) and interface | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:44 |
| S13 | 0 | ((((single adj2 chip) same core same peripheral same programmable) and timer) and interface) and (custom$3 adj2 peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:44 |
| S14 | 8 | ((((single adj2 chip) same core same peripheral same programmable) and timer) and interface) and ((single adj2 chip) same core same peripheral same programmable) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:45 |
| S15 | 0 | (custom$3 adj2 peripheral) and ((single adj2 chip) same core same peripheral same programmable) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:46 |
| S16 | 0 | (custom$3 adj2 peripheral) and (programmable adj2 chip) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:46 |
| S17 | 67 | custom$3 adj peripheral | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:46 |

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| S18 | 0 | uart and (custom$3 adj peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:46 |
| S19 | 0 | (singgle adj chip) and (custom$3 adj peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:47 |
| S20 | 5 | (single adj chip) and (custom$3 adj peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/09 09:47 |
| S21 | 44302 | (programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:08 |
| S22 | 834917 | parameter$5 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:09 |
| S23 | 13940 | parameter$6 same core | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:10 |
| S24 | 254847 | (peripheral or interface) and processor | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:12 |
| S25 | 14670 | ((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and parameter$5 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:12 |
| S26 | 455 | ((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:13 |
| S27 | 347 | ( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:13 |

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| S28 | 323 | implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:13 |
| S29 | 0 | configur%6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core)))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:14 |
| S30 | 303 | configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core)))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:14 |
| S31 | 158 | synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core))))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:15 |
| S32 | 158 | description and (synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core)))))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:15 |
| S33 | 135 | interconnect$3 and (description and (synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core))))))) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:16 |
| S34 | 477 | custom$6 adj4 peripheral | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:18 |

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| S35 | 0 | (interconnect$3 and (description and (synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core)))))))) and (custom$6 adj4 peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:17 |
| S36 | 0 | (description and (synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core))))))) and (custom$6 adj4 peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:17 |
| S37 | 15 | ((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (custom$6 adj4 peripheral) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:23 |
| S38 | 7 | parameter$5 and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (custom$6 adj4 peripheral)) | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:25 |
| S39 | 4615 | wizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:26 |
| S40 | 1 | (parameter$5 and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (custom$6 adj4 peripheral))) and wizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:27 |
| S41 | 244 | ((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and wizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:27 |

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| S42 | 11 | (description and (synthes$5 and (configur$6 and (implement$5 and (( (peripheral or interface) and processor) and (((programmable adj2 chip) or (programmable adj2 device) or (programmable adj2 logic)) and (parameter$6 same core))))))) and wizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/16 10:27 |
| S43 | 1 | wizard same integrated adj2 design | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 07:58 |
| S44 | 358 | wizard same parameter | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 07:59 |
| S45 | 0 | subwizard same spawn$3 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 07:59 |
| S46 | 4 | subwizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 08:02 |
| S47 | 2 | parameter and subwizard | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 09:46 |
| S48 | 0 | (device adj driver adj logic) same hdl | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 09:49 |
| S49 | 24 | device adj driver adj logic | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/07/21 09:49 |
| S50 | 773 | programmable adj chip | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:30 |

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| S51 | 130 | (processor adj2 core) same parameter | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:30 |
| S52 | 8797 | peripheral same parameter | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:31 |
| S53 | 21 | S51 and S52 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:39 |
| S54 | 0 | S50 and S53 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:31 |
| S55 | 13 | chip and S53 | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2004/11/30 16:40 |